UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,623	02/02/2001	Hiroyuki Kuzuma	49657-894	7719

7590 12/30/2004

McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
SHAAWAT, MUSSA	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 12/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,623	KUZUMA ET AL.	
	Examiner	Art Unit	
	Mussa A Shaawat	2128	

-- The MAILING DATE of this communicati n appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Ho, Patent No. (5,828,580) referred to hereinafter as Ho.

As per claim 1, Ho teaches a back annotation apparatus including, see **Ho** (Abstract): a pre-layout simulation implementing part for detecting nodes of which the potential changes when a predetermined signal is applied to a logic circuit, see **Ho** (col.5, lines 1-15); a layout pattern verification implementing part for implementing a predetermined layout pattern verification for layout patterns of the logical circuit, see **Ho** (col.4, lines 18-37); a parasitic element extraction part connected to the pre-layout simulation implementing part which extracts parasitic elements from the nodes of which the potential changes, see **Ho** (col.5, lines 27-55); a net list generation part connected to the parasitic element extraction part for generating a net list which includes all the devices included in the layout pattern data and parasitic elements extracted in the parasitic element extraction part; and a post layout simulation implementing part connected to the net list generation part for implementing a post layout simulation by using the net list, see **Ho** (col.6, lines 5-15, col.7, lines 49-63).

As per claim 2, Ho teaches a back annotation apparatus according to claim 1, wherein the pre-layout simulation implementing part includes: an active node detection part for detecting nodes of which the potential changes when a predetermined signal is applied to the logic circuit; and a non active node detection part for detecting nodes of which the potential does not change when the predetermined signal is applied to the logic circuit, see **Ho** (col.4, lines 60-67, col.5, lines 1-20), the net list generation part includes a net list generation part with parasitic elements which is connected to the parasitic element extraction part and the layout pattern verification implementing part and which generates a net list including parasitic elements to the active nodes within the layout pattern data and devices connected to the active nodes, the post layout simulation implementing part includes a circuit which is connected to the net list generation part and the non active node detection part, which fixes the potential of the node, of which the potential does not change, at a predetermined potential and which implements a post layout simulation by using the net list, see **Ho** (col.6, lines 5-15, col.7, lines 49-63).

As per claim 3, Ho teaches a back annotation apparatus according to claim 2 further including: an internal node extraction part for extracting layout pattern data or nodes of the logic circuit diagram which is connected to the layout pattern verification implementing part and to which serially connected devices degenerated according to a predetermined standard at the time of layout pattern verification are connected in parallel; and a node information updating part for updating the detection result of the active node detection part and the non active node detection part based on the extraction result at the internal node extraction part, which is connected to the internal node extraction part, the active node detection part and the non active node detection part, see **Ho** (col.7, lines 5-63, col.8, lines 5-17).

As per claim 4, claim 4 includes the same limitations of claim 3; therefore it is rejected based on the same rationale, supra.

As per claim 5, Ho teaches a back annotation apparatus according to claim 2 further including: a first internal node extraction part for extracting layout pattern data or nodes of the logic circuit diagram which is connected to the layout pattern verification implementing part and to which serially connected devices degenerated according to a predetermined standard at the time of layout pattern verification are connected in parallel; a second internal node extraction part for extracting layout pattern data or nodes of the logic circuit diagram which is connected to the layout pattern verification implementing part and wherein serially connected elements degenerated according to a predetermined standard at the time of layout pattern verification are made to be a single element, see **Ho** (col.8, lines 5-15); a node information updating part for updating the detection result of the active node detection part and the non active node detection part based on the extraction result at the first and the second internal node extraction parts, which is connected to the first internal node extraction part, the second internal node extraction part, the active node detection part and the non active node detection part; and a parasitic element information degenerating part for degenerating only the parasitic element information included in the net list which is connected to the net list generation part with parasitic elements, see **Ho** (col.7, lines 5-63, col.8, lines 5-17).

As per claims 6 –10, claims 6-10 include the same limitations of claims 1-5; therefore they are rejected based on the same reasoning, supra.

3. Applicant's arguments filed have been fully considered but they are not persuasive.

In the remarks, the applicant argues in substance that; A) Ho does not disclose a pre-layout simulation implementing part for detecting the nodes of which the potential changes when a predetermined signal is applied to a logic circuit, as claim 1 requires; or the step of detection of nodes of which the potential changes when a predetermined signal is applied to a logic circuit, as recited in claim 6; B) Ho does not disclose extracting parasitic elements from which the nodes of which the potential changes, as claims 1 and 6 require.

In response to applicant arguments, the examiner respectfully submits that Ho teaches a continuous net by net extraction as described in col.5 lines 1-6 and col.5 lines 15-20. By this continuous net-by-net extraction, Ho implicitly teaches the extraction of parasitic elements from the nodes at all times. This includes extracting node information after or before a potential change occurs at the node. Therefore, the disclosed continuous net-by-net extraction of parasitic elements of the layout of the integrated circuit (see col.5 lines 1-6 and lines 15-20) meets the scope of the claimed limitation whereby a pre-layout simulation that detects potential changes in nodes when a predetermined signal is applied to a logic circuit. It also meets the scope of extracting parasitic elements from the node of which the potential changes, as claims 1 and 6 require. Further, the examiner submits that Ho's teaching of having a user to select a node or nodes graphically for extraction see (col. 4 lines 62-65), meets the scope of the claimed limitation "implementing part for detecting nodes".

In light of the foregoing arguments, the 35 USC 102 rejection is hereby sustained.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Ho, US Patent No. (5,828,580) Connectivity based approach for extracting parasitic layout in an integrated circuit.
- Heile, US Patent No. (6,317,860) Electronic design automation tool for display of design profile.
- Raghavan et al, US Patent No. (6,286,126) Methods, and apparatus for post-layout verification of micro electric circuits using best and worst case delay models for nets therein.

- Rostoker et al, US Patent No. (5,933,356) methods and system for creating and verifying structural logic models of electronic design from behavioral description.
- Raghavan et al, US Patent No. (5,896,300) methods apparatus and computer program products for performing post-layout verification of micro electronic circuits by filtering timing error bounds for layout critical nets.
- Graef et al, US Patent No. (6,083,269) digital integrated circuit design system and methodology with hardware.
- Campmas et al, US Patent No. (5,717,928) system and method for obtaining a mask programmable device using a logic description and a field programmable device implementing the logic description.
- Sakai, US Patent No. (6,099,581) layout database for a computer aided design system.
- Smith, Jr. et al, US Patent No. (5,452,224) method of computing multi-conductor parasitic capacitances for VLSI circuits.
- Mc Connell et al, US 2001 Pub. No. (0049593 A1) software tool to allow field programmable system level devices.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mussa A Shaawat whose telephone number is (571) 272-3785. The examiner can normally be reached on Monday-Friday (8:30am to 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R Homere can be reached on (571) 272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mussa Shaawat
Patent Examiner
December 21, 2004

JEAN HOMERE
SUPERVISORY PATENT EXAMINER